12-21-99

Patent Application Transmittal

(only for new nonprovisional applications under 37 C.F.R. 1.53(b))

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Date: December 20, 1999
Attorney Docket No.: 450100-4465.1

ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Sir:

With reference to the filing in the United States Patent and Trademark Office of an application for patent in the name(s) of:

Takumi OKAUE, Yoshio KONDO

entitled:

EXTERNAL STORAGE APPARATUS AND CONTROL APPARATUS THEREOF, AND DATA TRANSMISSION/RECEPTION APPARATUS

X Continuing Application

X Continuation ___ Divisional ___ Continuation-in-Part (CIP) of prior application serial no. 09/086,788, filed May 28, 1998.

[Note: If priority under 35 U.S.C. 120 involves a series of respectively copending applications, then in this amendment identify each and its relationship to its immediate predecessor.]

___ The prior application is assigned of record to SONY CORPORATION.

The following are enclosed:

X Specification (17 pages)

X 6 Sheet(s) of Drawings

X 6 Claim(s) (including 2 independent claim(s))

___ This application contains a multiple dependent claim

X Our check for $ 760.00, calculated on the basis of the claims existing in the prior application (less any claims canceled herein) as amended by any enclosed preliminary amendment as follows:

Basic Fee, $760.00 ($380.00)	$ 760.00
Number of Claims in excess of 20 at $18.00 ($9.00) each:	-0-
Number of Independent Claims in excess of 3 at $78.00 ($39.00) each:	-0-
Multiple Dependent Claim Fee at $260.00 ($130.00)	-0-
Total Filing Fee	$ 760.00

___ Assignment Recording Fee $40.00 -0-

___ This application is being filed within the first month following the expiration of the term originally set therefor in the prior application. This is a petition to request a 1-month extension of time. A check covering the cost of the petition is enclosed.

Patent Application Transmittal

(only for new nonprovisional applications under 37 C.F.R. 1.53(b))

450100-4465.1

_X_ Oath or Declaration and Power of Attorney
___ New ___ signed ___ unsigned
_X_ Copy from a prior application (37 C.F.R. 1.63(d))

Deletion of Inventors

___ Signed Statement attached deleting inventor(s) named in the prior application (37 C.F.R. 1.63(d)(2) and 1.33(b))

Power of Attorney or Correspondence Address Change

_X_ Power of attorney and/or correspondence address was changed during prosecution of the prior application. The new power of attorney is to **William S. Frommer, Reg. No. 25,506** . The new correspondence address is indicated above.

_X_ Incorporation by Reference (for continuation or divisional application) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

_X_ A Preliminary Amendment is enclosed.
(Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

_X_ Cancel in this application original claims 2-18 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

_X_ New formal drawings are enclosed.

_X_ Certified copy of each foreign priority application on which the claim for priority under 35 U.S.C. 119 is based was filed in prior U.S. application serial no. 09/086,788, filed May 28, 1998. A list of said foreign priority application(s) is provided below. Acknowledgement thereof is requested.

Application No.	Filed	In
9-146913	4 June 1997	Japan

Please charge any additional fees required for the filing of this application or credit any overpayment to Deposit Account No. 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicants
WILLIAM S. FROMMER

By _____
Reg. No. 25,506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Continuation of Serial No. 09/086,788

Applicants	:	Takumi OKAUE, et al.
Filed	:	Herewith
For	:	EXTERNAL STORAGE APPARATUS AND CONTROL APPARATUS THEREOF, AND DATA TRANSMISSION/RECEPTION APPARATUS
Art Unit	:	2876

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Date of Deposit December 20, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Charles Jackson
(Typed or printed name of person mailing paper or fee)

Charles Jackson
(Signature of person mailing paper or fee)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

Sir:

Before the issuance of the first Official Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-18 and add the following new claims:

--19. A memory card for storing data transmitted from an external apparatus, said memory card comprising:

a flash memory for storing said data transmitted from said external apparatus;

a switch settable to a state which inhibits writing data into said flash memory;

an interface for transmitting data to and receiving data from said external apparatus; and

control means for controlling said memory card in accordance with an instruction transmitted from said external apparatus, said control means sending to said external apparatus via said interface the state of said switch in response to an instruction transmitted thereto via said interface from said external apparatus.--

--20. A memory card as claimed in claim 19, wherein said interface includes nine connectors at least one of which transmits and receives data.--

--21. A memory card as claimed in claim 19, wherein said data is received from and transmitted to said external apparatus in serial form.--

--22. A system comprising a memory card and an external apparatus, wherein data is communicated therebetween,

said memory card comprising:

a flash memory for storing said data transmitted from said external apparatus;

a switch settable to a state which inhibits writing data into said flash memory;

an interface for transmitting data to and receiving data from said external apparatus; and

control means for controlling said memory card in accordance with an instruction transmitted from said external apparatus, said control means sending to said external apparatus via said interface the state of said switch in response to an instruction transmitted thereto via said interface from said external apparatus;

and said external apparatus comprising:

a controller for writing data to or erasing data from the flash memory of said memory card, said controller transmitting an instruction to said memory card via said interface to determine whether a data writing operation to the flash memory of said memory card in inhibited.--

--23. A system as claimed in claim 22, wherein said interface includes nine connectors at least one of which transmits and receives data.--

--24. A system as claimed in claim 22, wherein said data is received from and transmitted to said external apparatus in serial form.--

REMARKS

This preliminary amendment adds claims directed to subject matter disclosed, but not claimed, in parent application 09/086,788. No new matter is added. Entry of the above amendatory matter and early examination on the merits are respectfully requested.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicants

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PATENT
450100-4465

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

TITLE: EXTERNAL STORAGE APPARATUS AND CONTROL APPARATUS THEREOF, AND DATA TRANSMISSION/RECEPTION APPARATUS

INVENTORS: Takumi OKAUE, Yoshio KONDO

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S98P-0617**00

TITLE OF THE INVENTION

External Storage Apparatus and Control Apparatus Thereof, and Data Transmission/Reception Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a memory card having an erroneous erase preventing function and its control apparatus, and a data transmission/reception apparatus.

Description of the Prior Art

Conventionally, an external storage apparatus such as a magnetic tape, magnetic disc, optical disc, memory card and the like is used for storing a data from an electronic apparatus such as computer, digital still camera and the like. Especially, the memory card is widely used for its convenience for carrying and high transfer rate.

Similarly as a flexible disc, a memory card as an erroneous erase prevention switch for preventing an erroneous erase of a data stored. However, a conventional erroneous erase prevention switch is provided on a main plane of the card memory body and a user cannot operate the switch when the memory card is mounted on an electronic apparatus.

In this case, if the memory card is inserted into an electronic apparatus and the user find that the memory card is disabled for writing, the user cannot write a new data on a data already stored. The user should pull out the memory card

from the electronic apparatus, set the erroneous erase prevention switch to a writable mode, and again mount the memory card into the electronic apparatus. It has been desired to improve the switching operationability of the erroneous erase prevention switch.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a memory card capable of preventing an erroneous erase of a data stored or another data writing on the data stored, while enabling to freely set the erroneous erase prevention switch to a desired mode, and its control apparatus, and its data transmission apparatus.

In order to achieve the aforementioned object, the memory card according to the present invention is a memory card for storing a data transmitted from a control apparatus, the memory card including: storage means for storing a data from the control apparatus: a switch for setting whether to inhibit writing of a data in the storage means; and control means for controlling writing of the data transmitted from the control apparatus, on the storage means.

In the memory card, the switch can be switched even when the memory card is mounted on the control apparatus; and the control means decides a setting content of the switch when writing a data transmitted from the control apparatus and transmits a write enabled signal to the control apparatus unless the switch is set to a write disabled mode, and

transmits a write disabled signal to the control apparatus if the switch is set to a write disabled mode.

The memory card control apparatus according to the present invention is a memory card control apparatus for controlling write and read of a data into/from a memory card, including: storage means for storing a data to be transmitted to the memory card; and control means for controlling write-in and read-out of a data into/from the storage means.

The control means functions in such a manner for each data write it is decided whether the memory card is set to a data write disabled mode; when a write enabled signal is received from the memory card, a data stored in the storage means is read out and written on the memory card; and when a write disabled signal is received from the memory card, read out of the data from the storage means is interrupted.

The data transmission and reception apparatus according to the present invention is for carrying out a data transmission and reception between a control block and a memory card, wherein the memory card includes: first storage means for storing a data from the control block; a switch for setting to inhibit writing of a data to the first storage means; and first control means for controlling write-in and read-out of a data into/from the first storage means, whereas the control block includes second storage means for storing a data to be transmitted to the memory card and second control means for controlling a data write-in and read-out into/from the second storage means.

In the data transmission and reception apparatus, the memory card, when writing a data transmitted from the control block, decides the setting content of the switch. Unless the switch is set to a write disabled mode, a write enabled signal is transmitted to the control block, and if the switch is set to a write disabled mode, a write inhibit signal is transmitted to the control block, thus controlling writing of a data transmitted from the control block, in the first storage means. Moreover, the first control means, for each data, decides whether the memory card is set to the data write inhibit mode. When the control block receives a write enabled signal from the memory card, the data stored in the second storage means is read out and is written in the first storage means. When a write inhibit signal is received from the memory card, read out of the data from the second storage means is interrupted.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of a host computer according to the present invention.

Fig. 2 is a block diagram showing a configuration of a memory card according to the present invention.

Fig. 3 is an external perspective view of the aforementioned memory card.

Fig. 4 is an external perspective view of the aforementioned memory card.

Fig. 5 is a flowchart which explains an operation procedure of the host computer and the memory card.

Fig. 6 is a flowchart which explains an operation procedure of the host computer and the memory card.

Fig. 7 is another external perspective view of the aforementioned memory card.

Fig. 8 is another external perspective view of the aforementioned memory card.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Hereinafter, description will be directed to embodiments of the present invention with reference to the attached drawings.

The present invention can be applied to a host computer shown in Fig. 1 and a memory card for storing a data from this host computer. It should be noted that an embodiment will be explained for a case of writing a video data transmitted from the host computer, on a memory card, but the present invention can also be applied to a data other than a video data such as an audio data.

As shown in Fig. 1, the aforementioned host computer 1 includes: a hard disc 11 for storing various data such as a video data of a still image data and an audio data; a RAM (random access memory) 12 for temporarily storing and reading out the video data and other data from the hard disc 11; a display interface (hereinafter referred to as a display I/F) 13; a display 14 for display an image according to the video data supplied via the display interface 13; a serial interface (hereinafter, referred to as a serial I/F) 15 for transmitting

and receiving a data to/from a memory card 2 via three data lines; a bus 16; and a CPU (central processing unit) for the entire control.

The RAM 12, for example, temporarily stores a video data stored in the hard disc 11 via the bus 16 and, when necessary, supplies the video data via the bus 16 to the serial I/F 15.

The display 14 is supplied via the bus 16 and the display I/F 13 with the video data which has been read out from the hard disc 11 or a video data from the memory card 2, so that a still image or a moving picture is displayed according to these video data.

The serial I/F transmits a video data to the memory card 2 or receives a video data stored in the memory card 2 via the three data lines. More specifically, via a first data line, the serial I/F 15 transmits a video data and a control data for writing into the memory card 2 and receives a video data read out from the memory card 2. Via a second data line, the serial I/F 15 outputs a state signal indicating a state switched according to the image data or control data supplied via the first data line. Furthermore, via a third data line, the serial I/F 15 transmits a serial clock SCLK for transmission of the aforementioned control data and video data.

The CPU 17 controls reading out of a video data from the RAM 12 and the hard disc 11 and writing of a video data into the RAM 12 as well as controls transmission and reception of a video data to/from the memory card 2. For example, the CPU 17 issues a register instruction to decide whether a write

protect of an erroneous erase prevention switch which will be detailed later is in ON state, and issues to the memory card 2 a write instruction for writing a predetermined video data with specification of an address.

On the other hand, as shown in Fig. 2, the memory card 2 includes: a control IC 21 for receiving a video data and a control data from the aforementioned host computer 1; a flash memory for storing the video data; and an erroneous erase prevention switch 23 for preventing an erroneous erase of the video data stored in the flash memory 22.

As shown in Fig. 3, the control IC 21, the flash memory 22, and the erroneous erase prevention switch 23 are provided in a plate-shaped member 24 formed almost in a plate shape. The erroneous erase prevention switch 23 is provided at one end of the longitudinal direction of the plate-shaped member 24, which end is opposite of the mounting direction. The erroneous erase prevention switch 23 is slidable in a direction intersecting at a right angle with the longitudinal direction of the plate-shaped member 24. When the erroneous erase prevention switch 23 is set at a left position viewed toward the mounting direction as shown in Fig, 3, it is possible to record a video data, i.e., the write protect is in OFF state.

Moreover, as shown in Fig. 4, when the erroneous erase prevention switch 23 is at a right position viewed toward to mounting direction, a cut-off portion 25 can be seen. In this state, the memory card 2 is disabled for recording a video data. That is, the write protect is in ON state.

Consequently, a user can know the state of the memory card 2 by touching it with a finger, i.e., whether the write protect is ON or OFF through presence or absence of the aforementioned cut-off portion 25 even when the memory card 2 is placed in pocket of a jacket.

The control IC 21, prior to writing a video data from the host computer 1 into the flash memory 22, decides whether the erroneous erase prevention switch 23 is set to write protect ON or OFF state, so that the video data is written in the flash memory 22 only when the write protect is OFF.

Here, more specifically, the control IC 21 includes: a serial/parallel - parallel/serial interface sequencer (hereinafter, referred to as an S/P & P/S sequencer) 31; a page buffer 32 for temporarily storing a video data from the S/P & P/S sequencer; a flash interface sequencer (hereinafter, referred to as a flash I/F sequencer) 33 for supplying the video data from the page buffer 32, to the flash memory 22; an ECC encoder/decoder 34 for carrying out an error correction processing; a command generator 35 for generating a predetermined control command; a configuration ROM (read only memory) 36 containing a version information and others; and an oscillator 37 of supplying a clock to respective circuits.

the S/P & P/S sequencer 31 is connected via the aforementioned first to third data lines to the serial I/F 15 of the host computer 1. Thus, the S/P & P/S sequencer 31 is supplied from the host computer 1 with a status signal and a serial clock SCLK as well as a serial data DIO consisting of

a video data and a control data.

The S/P & P/S sequencer 31 converts the serial data DIO supplied from the host computer 1, into a parallel data in synchronization with the aforementioned serial clock SCLK. Among the parallel data, for example, the S/P & P/S sequencer 31 supplies a control data to the command generator 35 and a video data to the page buffer 32.

The page buffer is a buffer memory for storing the video data supplied from the S/P & P/S sequencer 31 on page (=512 bytes) basis. The video data stored in the page buffer 32 is added with an error correction code by the ECC encoder/decoder 34. The page buffer 32 supplied one page of video data added with the error correction code, via the flash I/F sequencer 33 to the flash memories 33a to 22d. Thus, the video data from the host computer 1 is written in the flash memories 22a to 22d.

Moreover, the image data read out from the flash memories 22a to 22d is supplied via the flash I/F sequencer 33 to the page buffer 32.

The page buffer 32 stores the video data from the flash I/F sequencer 33. Here, the ECC encoder/decoder 34 carries out an error correction processing according to the error correction code added to the data stored in the page buffer 32. The page buffer 32 reads out the data which has been subjected to the error correction processing page after another and supplies the data to the S/P & P/S sequencer 31. The S/P & P/S sequencer 31 converts the parallel video data supplied from the

page buffer 32, into a serial data DIO, and transmits it to the aforementioned host computer 1.

The command generator 35 generates a control command according to a control data from the S/P & P/S sequencer 31. For example, when the command generator 35 receives a read status register instruction for checking the operation state of the memory card 2, the setting mode of the erroneous erase prevention switch 23 is determined and according to this setting mode, it is determined whether to carry out writing of a video data.

Moreover, the command generator 35 generates a busy command (hereinafter, referred to as a busy signal) indicating that a video data is being written into the flash memory 22 or a video data is being read out from the flash memory 22, and transmits the busy command via the S/P & P/S sequencer 31 to the host computer 1. When the writing or reading of a video data is complete, the command generator 35 generates a ready command (hereinafter, referred to as a ready signal) indicating the writing or reading end, and transmits the ready command via the S/P & P/S sequencer 31 to the host computer 1. The host computer 1 recognizes the operation state of the memory card 2 by receiving these busy signal and ready signal.

The configuration ROM 36 contains a version information and an information of an initial value of the memory card 2. Consequently, when a connection is made between the host computer 1 and the memory card 2, the command generator 35 firstly reads out the aforementioned version information or the

like from the configuration ROM 36 via the S/P & P/S sequencer and generates a predetermined command according to the information, thus executing a predetermined initialization of the memory card 2.

In the host computer 1 and the memory card 2 having the aforementioned configuration, when a video data of the host computer 1 is written into the memory card 2, as shown in Fig. 5, the host computer execute a processing of steps S1 to S8 while the memory card 2 executes the processing of steps S11 to S14.

In the host computer 1, when a video data writing to the memory card 2 is specified, the CPU 17 issues a read status register instruction to check the state of the memory card 2 (step S1) and transmits this register instruction via the serial I/F 15 to the memory card 2. This read status register instruction is issued for each of the files to be transmitted.

In the memory card 2, when the command generator 35 receives the aforementioned register instruction via the S/P & P/S sequencer 31, the state of the erroneous erase prevention switch 23 is set to a register mode, and the contents of this register is transmitted via the S/P & P/S sequencer 31 to the host computer 1 (step S11). In other words, the command generator 35 decides whether the erroneous erase prevention switch is ON, i.e., whether the write protect of the memory card 2 is ON, sets the state in the register and transmits this register content to the host computer 1.

In the host computer 1, the CPU 17, according to the

register content from the memory card 2, decides whether the write protect is ON (step S2) and if the write protect is ON, carries out a write inhibit processing (step S3).

When the CPU 17 decides that the write protect is not ON, the CPU 17 issues a write page buffer instruction and reads out a video data of 512 bytes from the hard disc 11, for example, and transmits the write page buffer instruction and the video data via the serial I/F 15 to the memory card 2 (step S4).

Furthermore, the CPU 17 issues a set command instruction and issues a write instruction with specification of a write address of the aforementioned data on the memory card 2 (step S5). The CPU 17 transmits these command instructions via the serial I/F 15 to the memory card 2.

In the memory card 2, when the command generator 35 receives the set command instruction from the host computer 1 via the S/P & P/S sequencer 31, the command generator sets a busy state in the register and transmits a busy signal indicating this register content, via the S/P & P/S sequencer 31 to the host computer 1 (step S12). It should be noted that his busy signal is repeatedly transmitted to the host computer 1 until the ready state is set in the register.

Moreover, the command generator 35 issues a command for executing writing so as write one page of the video data in the aforementioned specified address of the flash memory 22 (step S13). When the writing of the one page of video data is complete, the command generator 35 sets a ready state in the register and transmits a ready signal indicating this register

content, via the S/P & P/S sequencer 31 to the host computer 1 (step S14).

On the other hand, in the host computer 1, the CPU 17 issues the set command instruction in the aforementioned step S5 and after this, issues a read status register instruction to check the state of the memory card 2 (step S6). The CPU 17 decides whether the signal transmitted from the memory card 2 via the serial I/F 5 is a busy signal. If the signal is found to be a busy signal, the CPU 17 again issues the read status register instruction (step S6). That is, while the busy signal is transmitted from the memory card 2, the processing of steps S6 and S7 is repeatedly executed.

When the CPU 17 decides that the signal transmitted from the memory card 2 is not a busy signal, i.e., that the signal transmitted is a ready signal, the CPU 17 decides whether a subsequent video data to be transmitted to the memory card 2 is present. If a subsequent video data is present, control is passed to step S4, and if no subsequent video data is present, the transmission of video data is terminated (step S8). That is, a file of video data to be recorded is written on page basis into the memory card 2 by repeating the processing of steps S4 to S8 and the processing of steps S12 to S14.

As has been described above, according to the present invention, the ON/OFF state of the write protect of the memory card 2 is decided for each file recording. Consequently, if the write protect setting is changed by the erroneous erase prevention switch 23 while the memory card 2 is mounted on the

host computer 1, it is possible to carry out a processing to inhibit the video data writing or record the video data according to the set content.

Moreover, the erroneous erase prevention switch 23 can be changed in the write protect setting while the memory card is mounted on the host computer 1, and accordingly there is no need of removal of the memory card 2 from the host computer 1 for switching the erroneous erase prevention switch 23, thus improving the operationability for the user.

Next, description will directed to the operation when erasing a video data stored in the memory card 2. When erasing a video data stored in the memory card 2, as shown in Fig. 6, the host computer 1 carries out a processing of steps S21 to S27 while the memory card 2 carries out a processing of steps S31 to S34.

In the host computer 1, when an erase is set for a video data stored in the memory card 2, the CPU 17 issues a read status register instruction (step S21) so as to check the state oft he memory card 2, and transmits this register instruction via the serial I/F 15 to the memory card 2. It should be noted that this read status register instruction is issued for each of the files to be transmitted.

In the memory card 2, when the command generator 35 receives the aforementioned register instruction, the command generator 35 sets the state of the erroneous erase prevention switch 23 in a register, and transmits this register content via the S/P & P/S sequencer 31 to the host computer 1 (step

S31). In other words, the command generator 35 set in register the ON or OFF state of the write protect of the memory card and transmits this register content to the host computer 1.

In the host computer 1, the CPU 17 decides whether the write protect is ON according to the register content from the memory card 2 (step S22) and if the write protect is ON, a processing to inhibit erase is carried out (step S23).

Moreover, the CPU 17 issues a set command instruction, and with specification of an address of the video data to be erased, issues an erase instruction (step S24). The CPU 17 transmits these command instructions via the serial I/F 15 to the memory card 2.

On the other hand, in the memory card 2, the command generator 35, upon reception of the aforementioned set command instruction from the host computer 1, transmits a busy signal via the S/P & P/S sequencer 31 to the host computer 1 (step S32).

Moreover, the command generator 35 issues a command to erase the video data of the specified address, so as to erase the specified video data stored in the flash memory 22 (step S33). It should be noted that in the flash memory 22, the video data is erased for each block consisting of a predetermined number of sets of one-page (512 bytes) video data and 18-byte of management information.

When the aforementioned erase of the video data is complete, the command generator 35 sets a ready state in the register and transmits a ready signal indicating the register

content, via the S/P & and P/S sequencer 31 to the host computer 1 (step s34).

On the other hand, in the host computer 1, the CPU 17 issues the set command instruction in the aforementioned step S24 and after this, issues a read status register instruction to check the state of the memory card 2 (step S25). The CPU 17 decides whether a signal transmitted from the memory card 2 via the serial I/F 15 is a busy signal. If the signal is a busy signal, the read status register instruction is again issued (step S26). Consequently, while the busy signal is transmitted from the memory card 2, the processing of steps S25 and S26 is repeatedly carried out.

When the CPU 17 decides that the signal transmitted from the memory card 2 is not a busy signal, i.e., the signal transmitted is a ready signal, the CPU 17 decides whether any video data to be erased is present in the memory card 2. If any subsequent data to be erased is present, control is passed to step S24, and if no video data to be erased is present, the video data erase is terminated (step S27). That is, the file of video data to be erased is erased on block basis by repeatedly carrying out the aforementioned procedure of steps S24 to S27 and steps S32 to S34.

As has thus far been described, according to the present invention, the ON/OFF state of the write protect of the memory card 2 is checked for each file erase and if the write protect setting is changed by the erroneous erase prevention switch 23 while the memory card 2 is mounted on the host computer 1, it

is possible to carry out a processing to inhibit erase of the video data according to the set content.

It should be noted that the present invention is not to be limited to the aforementioned embodiment but can be modified in various designs within the scope of the present invention.

For example, the erroneous erase prevention switch 23 can be modified in any ways if it is provided at one end of the longitudinal direction of the plate-shaped member 24 and is slidable on the direction intersecting the aforementioned longitudinal direction at a right angle. Consequently, as shown in Fig. 7 and Fig. 8, it is possible to provide the erroneous erase prevention switch 23 on the main plane of the plate-shaped member 24. In this case, as shown in Fig. 7, when the erroneous erase prevention switch 23 is placed at the left side viewed toward the mounting direction, the write protect is set to OFF. Moreover, as show in Fig. 8, when the erroneous erase prevention switch 23 is positioned at the right side viewed toward the mounting direction, a vacancy 26 can be seen. In this state, it is possible to turn the write protect ON. Consequently, the user can know whether the vacancy 26 is present, i.e., whether the write protect is ON or OFF by touching the erroneous erase prevention switch 23 with a finger even if the memory card 2 is placed in a pocket of his/her jacket.

WHAT IS CLAIMED IS

1. A memory card for storing a data transmitted from a control apparatus, said memory card comprising:

storage means for storing a data from said control apparatus:

a switch for setting whether to inhibit writing of a data in said storage means; and

control means for controlling writing of the data transmitted from said control apparatus, on said storage means,

wherein

said switch can be switched even when said memory card is mounted on said control apparatus; and

said control means decides a setting content of said switch when writing a data transmitted from said control apparatus and transmits a write enabled signal to said control apparatus unless said switch is set to a write disabled mode, and transmits a write disabled signal to said control apparatus if said switch is set to a write disabled mode.

2. A memory card as claimed in Claim 1, wherein said switch is provided on a rear end of a mounting direction of said memory card on said control apparatus.

3. A memory card as claimed in Claim 1, wherein said switch is formed so as to be slidable and is set to a write disabled mode when it is moved to one direction and is set to a write enabled mode when it is moved to the other direction;

and

when said write disabled mode is set in, there is a vacant portion apparent between said slide switch and said memory card.

4. A memory card for storing a data transmitted from a control apparatus, said memory card comprising:

storage means for storing a data from said control apparatus;

a switch for setting whether to inhibit writing a data on said storage means; and

control means for controlling erase of a data stored in said storage means;

wherein

said switch can be switched over even when said memory card is mounted on said control apparatus; and

said control means decides a setting content of said switch when erasing a data transmitted from said control apparatus and transmits a write enabled signal to said control apparatus unless said switch is set to a write disabled mode, and transmits a write disabled signal to said control apparatus if said switch is set to a write disabled mode.

5. A memory card as claimed in Claim 4, wherein said switch is provided on a rear end of a mounting direction of said memory card on said control apparatus.

6. A memory card as claimed in Claim 4, wherein said switch is formed so as to be slidable and is set to a write disabled mode when it is moved to one direction and is set to a write enabled mode when it is moved to the other direction; and

when said write disabled mode is set in, there is a vacant portion apparent between said slide switch and said memory card.

7. A memory card control apparatus for controlling write and read of a data into/from a memory card, said control apparatus comprising:

storage means for storing a data to be transmitted to said memory card; and

control means for controlling in such a manner that for each data write it is decided whether said memory card is set to a data write disabled mode; when a write enabled signal is received from said memory card, a data stored in said storage means is read out and written on said memory card; and when a write disabled signal is received from said memory card, read out of the data from said storage means is interrupted.

8. A control apparatus as claimed in Claim 7, wherein said control means decides whether said memory card is set to a data write disabled mode for writing of each file of data.

9. A memory card control apparatus for controlling

write-in and read-out of a data into/from a memory card, said apparatus comprising control means for controlling in such a manner that for each data erase it is decided whether said memory card is set to a data write disabled mode; when a write enabled signal is received from said memory card, a data stored in said storage means is erased; and when a write disabled signal is received from said memory card, erase of the data stored in said storage means is interrupted.

10. A memory card control apparatus as claimed in Claim 9, wherein said control means, when executing an erase of each file of data, decides whether said memory card is set to a data write disabled mode.

11. A data transmission and reception apparatus for carrying out a data transmission and reception between a control block and a memory card,

said memory card comprising:

first storage means for storing a data from said control block;

a switch for setting whether to inhibit writing of a data to said first storage means; and

first control means which decides a setting content of said switch when writing a data transmitted from said control block, in said first storage means, and transmits a write enabled signal to said control block so that a data transmitted from said control block is written in said first

storage means unless said switch is set to a write disabled mode, and transmits a write disabled signal to said control block if said switch is set to a write disabled mode,

said control block comprising:

second storage means for storing a data to be transmitted to said memory card; and

second control means for controlling in such a manner that for each data write it is decided whether said memory card is set to a data write disabled mode; when a write enabled signal is received from said memory card, a data stored in said second storage means is read out and written on said memory card; and when a write disabled signal is received from said memory card, read out of the data from said second storage means is interrupted.

12. A data transmission and reception apparatus as claimed in Claim 11, wherein said switch is provided on a rear end of a mounting direction of said memory card on said control apparatus.

13. A data transmission and reception apparatus as claimed in Claim 11, wherein said switch is formed so as to be slidable and is set to a write disabled mode when it is moved to one direction and is set to a write enabled mode when it is moved to the other direction; and

when said write disabled mode is set in, there is a vacant portion apparent between said slide switch and said memory

card.

14. A data transmission and reception apparatus as claimed in Claim 11, wherein said second control means decides whether said memory card is set to a data write disabled mode when carrying out write of one file of data.

15. A data transmission and reception apparatus for carrying out a data transmission and reception between a control block and a memory card,

said memory card comprising:

first storage means for storing a data from said control block;

a switch for setting whether to inhibit writing of a data to said first storage means; and

first control means which decides a setting content of said switch for each erasing of a data stored in said first storage means, and transmits a write enabled signal to said control block so that a predetermined data in said first storage means is erased according to a predetermined data erase instruction unless said switch is set to a write disabled mode, and transmits a write disabled signal to said control block if said switch is set to a write disabled mode,

said control block comprising:

second control means for controlling in such a manner that for each data erase it is decided whether said memory card is set to a data write disabled mode; when a write enabled

signal is received from said memory card, a predetermined data erase instruction is issued to said memory card; and when a write disabled signal is received from said memory card, issuance of said erase instruction to said memory card is interrupted,

wherein said switch can be switched over even when said memory card is mounted on said control block.

16. A data transmission and reception apparatus as claimed in Claim 15, wherein said switch is provided on a rear end of a mounting direction of said memory card on said control apparatus.

17. A data transmission and reception apparatus as claimed in Claim 15, wherein said switch is formed so as to be slidable and is set to a write disabled mode when it is moved to one direction and is set to a write enabled mode when it is moved to the other direction; and

when said write disabled mode is set in, there is a vacant portion apparent between said slide switch and said memory card.

18. A data transmission and reception apparatus as claimed in Claim 15, wherein said second control means decides whether said memory card is set to a data write disabled mode when carrying out write of one file of data.

ABSTRACT

The object of the present invention is to enable to prevent an erroneous erase of a data stored or writing another data on the data as well as to enable to easily switch an erroneous erase prevention switch.

A command generator 35, upon reception of a register instruction for checking a state of a memory card 2 received via an S/P & P/S sequencer, sets a state of an erroneous erase prevention switch 23 in a register and transmits this register content via the S/P & P/S sequnecer 31 to a host computer. According to the register content from the memory card, the host computer decides whether a write protect is ON and executes a write inhibit processing when the write protect is ON.

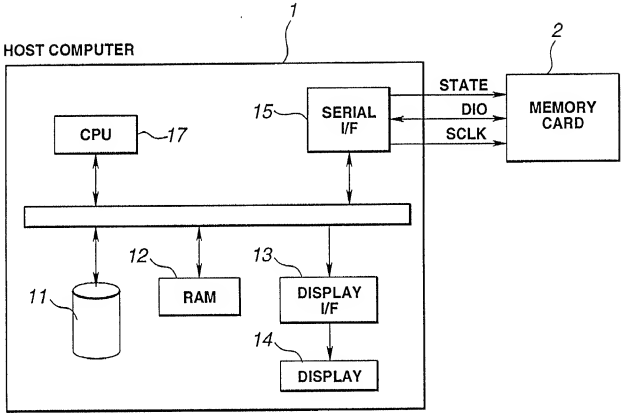
1
2
HOST COMPUTER
CPU
17
15
SERIAL I/F
STATE
DIO
SCLK
MEMORY CARD
12
RAM
13
DISPLAY I/F
11
14
DISPLAY

FIG.1

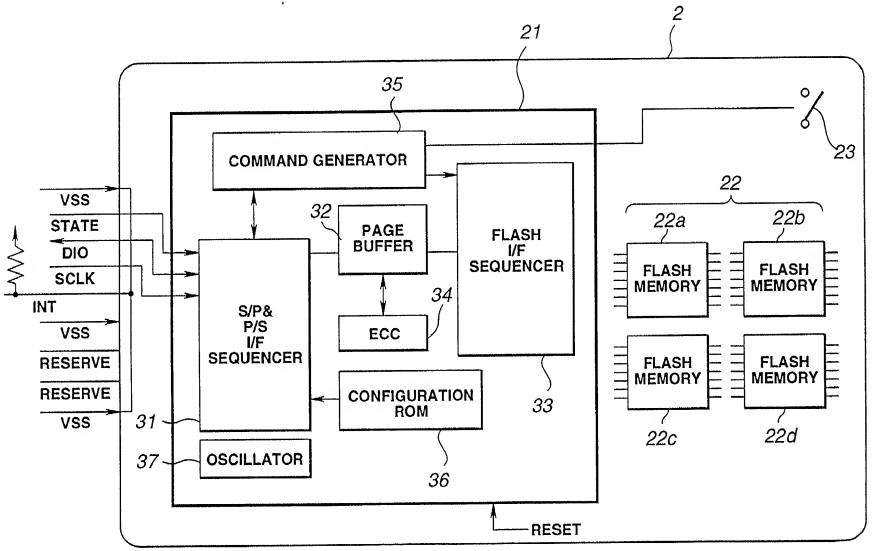
2
21
35
23
COMMAND GENERATOR
22
22a
22b
VSS
STATE
DIO
SCLK
INT
VSS
RESERVE
RESERVE
VSS
32
PAGE BUFFER
FLASH I/F SEQUENCER
FLASH MEMORY
FLASH MEMORY
34
ECC
S/P& P/S I/F SEQUENCER
CONFIGURATION ROM
33
FLASH MEMORY
FLASH MEMORY
31
37
OSCILLATOR
36
22c
22d
RESET

FIG.2

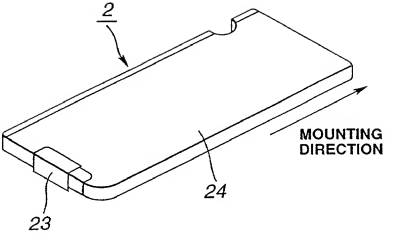

FIG.3

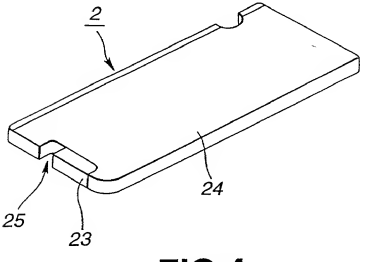

FIG.4

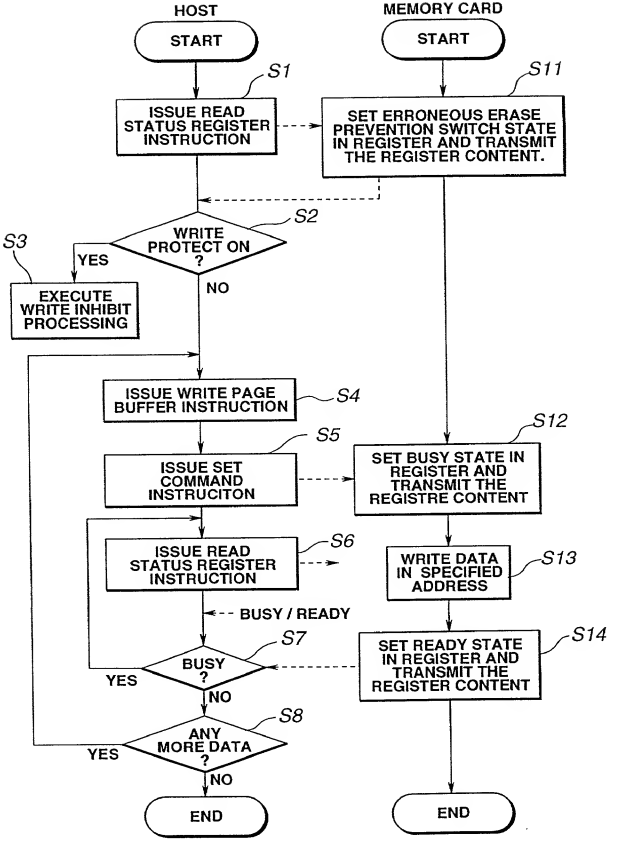
HOST
START
S1
ISSUE READ STATUS REGISTER INSTRUCTION
S2
WRITE PROTECT ON ?
YES
S3
EXECUTE WRITE INHIBIT PROCESSING
NO
ISSUE WRITE PAGE BUFFER INSTRUCTION
S4
S5
ISSUE SET COMMAND INSTRUCITON
ISSUE READ STATUS REGISTER INSTRUCTION
S6
BUSY / READY
S7
BUSY ?
YES
NO
S8
ANY MORE DATA ?
YES
NO
END
MEMORY CARD
START
S11
SET ERRONEOUS ERASE PREVENTION SWITCH STATE IN REGISTER AND TRANSMIT THE REGISTER CONTENT.
S12
SET BUSY STATE IN REGISTER AND TRANSMIT THE REGISTRE CONTENT
WRITE DATA IN SPECIFIED ADDRESS
S13
S14
SET READY STATE IN REGISTER AND TRANSMIT THE REGISTER CONTENT
END

FIG.5

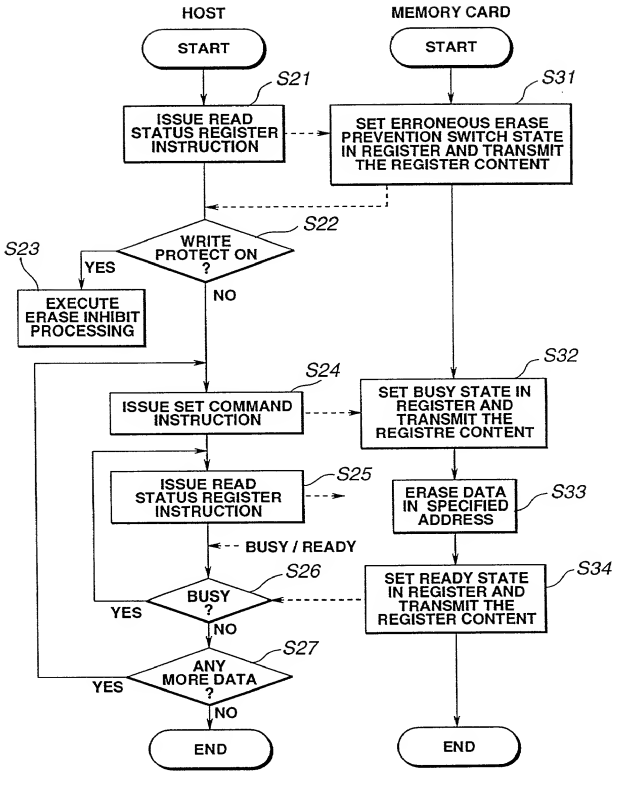
HOST
MEMORY CARD
START
START
S21
S31
ISSUE READ STATUS REGISTER INSTRUCTION
SET ERRONEOUS ERASE PREVENTION SWITCH STATE IN REGISTER AND TRANSMIT THE REGISTER CONTENT
S22
WRITE PROTECT ON ?
S23
YES
NO
EXECUTE ERASE INHIBIT PROCESSING
S24
S32
ISSUE SET COMMAND INSTRUCTION
SET BUSY STATE IN REGISTER AND TRANSMIT THE REGISTRE CONTENT
S25
ISSUE READ STATUS REGISTER INSTRUCTION
ERASE DATA IN SPECIFIED ADDRESS
S33
BUSY / READY
S26
S34
BUSY ?
SET READY STATE IN REGISTER AND TRANSMIT THE REGISTER CONTENT
YES
NO
S27
ANY MORE DATA ?
YES
NO
END
END

FIG.6

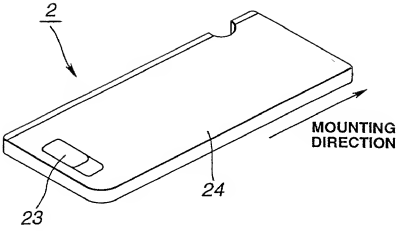

FIG.7

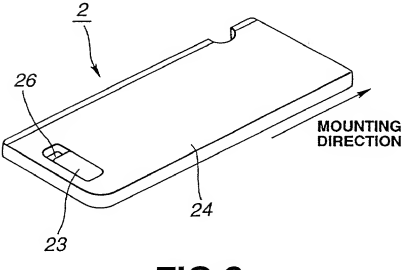

FIG.8

DECLARATION FOR PATENT APPLICATION (JOINT OR SOLE)
(Under 37 CFR § 1.63; with Power of Attorney)
FROMMER LAWRENCE & HAUG LLP

FLH File No. 450100-4465

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention ENTITLED:

EXTERNAL STORAGE APPARATUS AND CONTROL APPARATUS THEREOF, AND DATA TRANSMISSION/RECEPTION APPARATUS

the specification of which

____ is attached hereto.

__X__ was filed on __May 28, 1998__ as Application Serial No. __09/086,788__,

with amendment(s) through _____ (if applicable, give dates).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) [list additional applications on separate page]:			Priority Claimed:	
Number:	Country:	Filed (Day/Month/Year):	Yes	No
9-146913	Japan	4 June 1997	X	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s) [list additional applications on separate page]:		
Appln. Ser. Number:	Filed (Day/Month/Year):	Status (patented, pending, abandoned):

I hereby appoint __WILLIAM S. FROMMER__, Registration No. __25,506__, and __DENNIS M. SMID__, Registration No. __34,930__ or their duly appointed associate, my attorneys, with full power of substitution and revocation, to prosecute this application, to make alterations and amendments therein, to file continuation and divisional applications thereof, to receive the Patent, and to transact all business in the Patent and Trademark Office and in the Courts in connection therewith, and specify that all communications about the application are to be directed to the following correspondence address:

__WILLIAM S. FROMMER__, Esq.
c/o FROMMER LAWRENCE & HAUG LLP
745 Fifth Avenue
New York, New York 10151

Direct all telephone calls to:
(212) 588-0800
to the attention of:
__WILLIAM S. FROMMER__

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: Yoshio Kondo Date: August 5, 1998
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Citizenship: Japan

Signature: _____ Date: _____
Full name of 3rd joint inventor (if any):
Residence:
Citizenship:

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Post Office Address(es) of inventor(s):
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Note: In order to qualify for reduced fees available to Small Entities, each inventor and any other individual or entity having rights to the invention must also sign an appropriate separate "Verified Statement (Declaration) Claiming [or Supporting a Claim by Another for] Small Entity Status" form [e.g. for Independent Inventor, Small Business Concern, Nonprofit Organization, individual Non-Inventor].
Note: A post office address must be provided for each inventor.